AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (original) An apparatus for capturing and digitizing at least one analog signal derived from an event with a signal duration that is short compared to the interval between consecutive events, comprising:

two or more memories, each capable of storing a sequence of analog samples from one of two or more analog signals derived from the event;

a trigger for triggering the sampling and storage in the two or more memories of a sequence of analog samples to occur at about a 0.5 gigahertz or higher sampling rate;

means communicating with the memories for selectively initiating the read out of the analog samples in the memories;

an analog to digital converter for receiving each analog sample read out from each of memories and producing from the analog samples corresponding digitized sample values;

a digital signal processor for operably controlling parameters of the analog to digital converter and receiving the digitized sample values; and

an output stage under control of the digital signal processor for outputting the digitized sample values, such that the receiving and conversion and the output of digitized sample values are completed during the interval between consecutive events.

2. (original) The apparatus of claim 1 wherein the memories, digital signal processor and analog to digital converter are all integrated on one chip.

3. (original) The apparatus of claim 2 wherein the chip is a CMOS or bi-CMOS chip.

4. (original) The apparatus of claim 1 further comprising control software for the digital signal processor to select which memories to read out and in what order.

5. (original) The apparatus of claim 1 further comprising control software for the digital signal processor for pre-processing the digitized sample output values before they are output from the apparatus.

6. (currently amended) The apparatus of claim 1 wherein the digital signal processor operably controls one or more operating parameters of the trigger~~/input module~~.

7. (original) The apparatus of claim 1 wherein the digital signal processor operably controls one or more of the following operating parameters of the trigger: enable/disable trigger, selection of trigger source, setting trigger gain, clearing a triggered condition, setting the trigger threshold level and asserting the trigger action.

8. (original) The apparatus of claim 1 further comprising an input signal unit, wherein the digital signal processor operably controls one or more of the following operating parameters of the input signal unit: adjusting input level with an offset, adjusting input level with gain or attenuation, selecting the input source, setting an offset level, setting a gain or attenuation level.

9. (original) The apparatus of claim 1 further comprising an input signal unit, wherein the digital signal processor calibrates a gain level for the input signal unit.

10. (original) The apparatus of claim 1 further comprising an input signal unit, wherein the digital signal processor calibrates a gain level for the input signal unit by using a test signal unit to generate an input for the input signal unit with a known level.

11. (original) The apparatus of claim 1 further comprising an input signal unit, wherein the input signal unit senses an out of range condition in an input signal and sets a flag accessible to the digital signal processor for reading and clearing.

12. (currently amended) The apparatus of claim 1 further comprising a sampling timing unit wherein the digital signal processor operably controls one or more operating parameters of the sampling timing unit.

13. (currently amended) The apparatus of claim 1 further comprising a sampling timing unit wherein the digital signal processor operably controls one or more of the following operating parameters of the sampling timing unit: a rate of sample strobe generation and duration of the sampling period for one or more analog samples.

14. (currently amended) The apparatus of claim 1 further comprising a sampling timing unit wherein the digital signal processor operably controls one or more operating parameters of the sampling timing unit and calibrates the sampling rate.

15. (currently amended) The apparatus of claim 1 wherein each of the two or more memories comprises a matrix of capacitors defining one or more channels and the ~~DSP~~ digital

signal processor operably controls the selection of one or more channels for processing by the analog to digital converter.

16. (original) The apparatus of claim 1 further comprising a conversion unit wherein the digital signal processor operably controls one or more operating parameters of the conversion unit.

17. (currently amended) The apparatus of claim 1 further comprising a conversion unit with a comparator and a voltage reference that can be ramped wherein the digital signal processor operably controls one or more of the following operating parameters of the conversion unit: setting the comparator voltage level, resetting the ramp, starting the ramp, controlling the ramp speed, starting the counter for ramp levels, advancing the counter for ramp levels, setting the range over which the counter will count and ~~rest~~ resetting the counter.

18. (currently amended) The apparatus of claim 1 further comprising a readout unit in the output stage wherein the digital signal processor operably controls one or more operating parameters of the readout unit.

19. (original) The apparatus of claim 1 further comprising means in the digital signal processor for determining cell-to-cell result variations in sampling cells in the one or more memories, said digital signal processor applying corrections for the cell-to-cell result variations to the digitized sample values before outputting them.

20. (currently amended) The apparatus of claim 1 wherein one or more of the memories, the trigger~~/input module~~, the means for communicating with the memories for selectively

initiating readout, the analog to digital converter and the digital signal processor have low power modes and the digital signal processor operably controls the initiation and removal of the low power modes.

21. (original) The apparatus of claim 1 further comprising a timing generator for timing sampling and the timing generator is formed by a tapped delay line.

22. (currently amended) The apparatus of claim 1, wherein the analog to digital converter for receiving each analog sample read out from each of the memories is configured with multiple converters to act in parallel on the analog samples in a memory to produce corresponding digitized sample values.

23. (original) The apparatus of claim 1, wherein the analog to digital converter has a conversion unit with a ramped reference value and the digital signal processor calibrates a ramp speed for the converter.

24. (original) A method for capturing and digitizing analog signals derived from an event with a signal duration that is short compared to the interval between consecutive events comprising:

storing at about a 0.5 gigahertz or higher rate in each of two or more memories analog samples of one of two or more analog signals derived from the event;

selectively initiating the read out of the analog samples in memories;

receiving at an analog to digital converter each analog sample read out from at least one of the memories and producing for the analog samples in the at least one memory corresponding digitized sample values;

controlling the parameters of the analog to digital converter by use of a digital signal processor communicating with the analog to digital converter; and

outputting the digitized sample values under control of the digital signal processor, such that the receiving and conversion and the output of digitized sample values is completed during the interval between consecutive events.

25. (original) The method of claim 24 wherein the step of outputting the digitized sample values comprises outputting the digitized sample values from a port of the digital signal processor.

26. (original) The method of claim 24 further comprising testing analog samples in two or more of the memories and based on such testing the digital signal processor selecting which memories the analog to digital converter reads out and in what order.

27. (original) The method of claim 24 further comprising defining an input signal range and comparing the analog samples in each of the one or more memories to the input signal range, wherein the digital signal processor controls the analog to digital converter to convert only the analog samples of the memory whose analog samples most closely match the input signal range.

28. (original) The method of claim 24 further comprising the digital signal processor pre-processing the digitized sample values before these are outputted under control of the digital signal processor.

29. (original) The method of claim 24 further comprising pre-processing the digitized sample values to produce control information derived from the digitized sample values and outputting the control information with the digitized sample values.

30. (original) An apparatus for capturing and digitizing analog samples derived from a waveform representing an event, said waveform having a portion of interest for sampling with a duration that is short compared to the interval between waveforms comprising:

two or more memories each capable of storing analog samples from the waveform, sampled at approximately a 0.5 gigahertz or higher rate, said analog samples characterizing a substantial portion of a decay curve;

a digital signal processor;

control means associated with the digital signal processor for communicating with the memories and for selectively initiating the read out of the analog samples in memories;

an analog to digital converter for receiving analog samples read out from each of the memories and producing for each memory corresponding digitized sample values; and

an output stage under control of the digital signal processor for outputting the digitized sample values, such that the receiving and conversion and the output of digitized sample values is completed during the interval between consecutive signals.

31. (currently amended) The apparatus of claim 30, wherein the analog to digital converter for receiving each analog sample read out from each of the memories is configured with multiple converters to act in parallel on the analog samples in a memory to produce corresponding digitized sample values.

32. (original) An apparatus for capturing and digitizing at least one analog signal derived from an event, the signal duration for sampling being short compared to the interval between consecutive analog signals comprising:

at least one memory capable of storing a sequence of analog samples of the at least one analog signal derived from the event;

a trigger for triggering the sampling and storage in the at least one memory of a sequence of analog samples to occur at about a 0.5 gigahertz or higher rate;

a digital signal processor communicating with the at least one memory for selectively initiating the read out of the analog samples in the at least one memory;

an analog to digital converter for receiving analog samples read out from the at least one memory and producing from the analog samples corresponding digitized sample values;

means at the digital signal processor for receiving the digitized sample values and performing preprocessing to produce a digitized sample record; and

an output stage under control of the digital signal processor for outputting the digitized sample record, such that the receiving and conversion and the output of digitized sample record is completed during the interval between consecutive analog signals.